19-3581; Rev 0; 1/05

# Low-Voltage, 0.31Ω, Quad-SPDT Analog Switch



## General Description

The MAX4735 quad-SPDT switch routes audio signals in portable applications. Each channel has a 0.31Ω typical on-resistance, allowing the MAX4735 to drive 8Ω loudspeakers with less than 0.02% distortion.

The MAX4735 is configured as a quad-SPDT switch with two common control inputs. Each digital input controls two pairs of SPDT switches. The switches are fully bidirectional, allowing both multiplexing and demultiplexing operation. Break-before-make operation is guaranteed.

The device operates from a +1.6V to +3.6V supply and over the extended -40°C to +85°C temperature range. It is offered in both 16-pin 3mm x 3mm TQFN and TSSOP packages.

## Features

- **Low 0.31Ω $R_{ON}$**
- **0.06Ω On-Resistance Flatness**
- **Excellent 0.015Ω On-Resistance Matching**
- **Low 0.02% THD into 8Ω**
- **Low 0.015% THD into 32Ω**
- **Audio Signal Routing**
- **Space-Saving, 3mm x 3mm TQFN Package**
- **1.8V Logic Compatible**

## Applications

Cell Phones

Digital Still Cameras

PDAs and Palmtop Devices

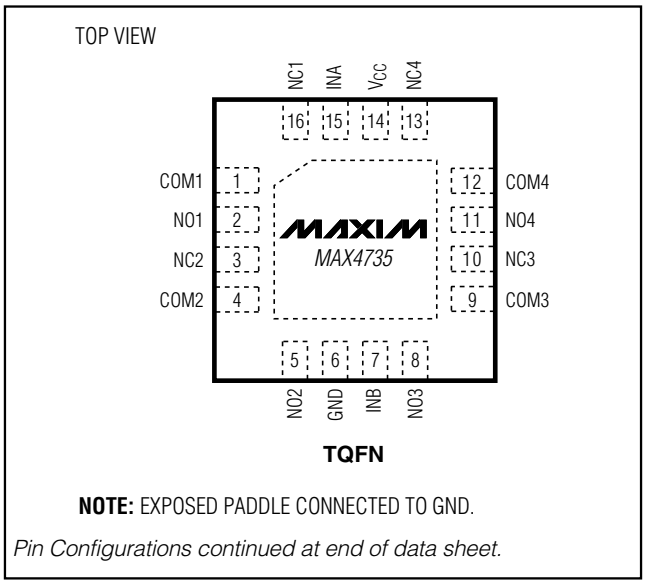
MP3 Players

## Ordering Information

| PART | PIN-PACKAGE | TOP MARK | PKG CODE |
|---|---|---|---|
| MAX4735ETE | 16 TQFN | ACT | T1633-4 |
| MAX4735EUE | 16 TSSOP | — | U16-2 |

***Note:*** *All products specified across the -40°C to +85°C temperature range.*

## Pin Configurations

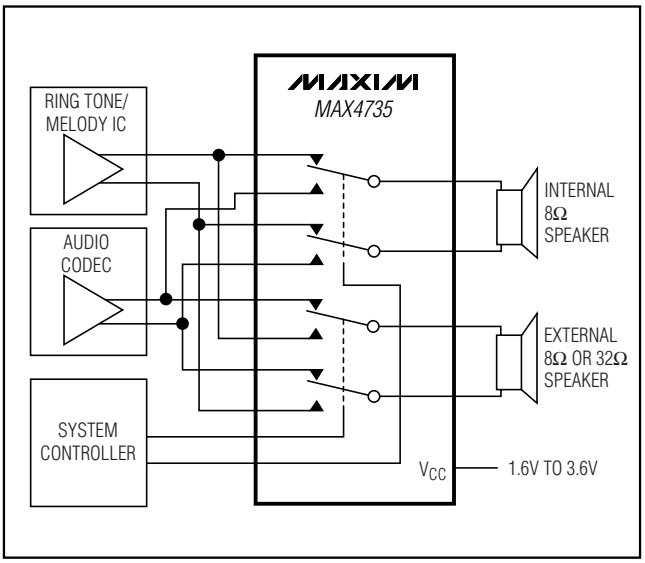



**TQFN**

**NOTE:** EXPOSED PADDLE CONNECTED TO GND.

*Pin Configurations continued at end of data sheet.*

## Typical Application Circuit






***For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.***

# Low-Voltage, 0.31Ω, Quad-SPDT Analog Switch

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$, INA, INB to GND .....-0.3V to +4.0V
All Other Pins to GND (Note 1).....-0.3V to ($V_{CC}$ + 0.3V)
Continuous Current (NO_, NC_, COM_)..... ±300mA
Peak Current (NO_, NC_, COM_)
(pulsed at 1ms, 50% duty cycle).....±400mA
Peak Current (NO_, NC_, COM_)
(pulsed at 1ms, 10% duty cycle .....±500mA

Continuous Power Dissipation ($T_A$ = +70°C)
16-Pin TQFN (derate 15.6mW/°C above +70°C) .....1.25W
16-Pin TSSOP (derate 9.4mW/°C above +70°C) .....755mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

**Note 1:** Signals on NO_, NC_, COM_ exceeding $V_{CC}$ or GND are clamped by internal diodes. IN_ is clamped to GND by an internal diode. Limit forward-diode current to maximum current rating.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 2.7V to 3.6V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = 3V, $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| Supply Voltage Range | $V_{CC}$ | | | 1.6 | | 3.6 | V |
| Supply Current | $I_{CC}$ | $V_{CC}$ = 3.6V, $V_{IN_}$ = 0 or $V_{CC}$, NO_ = NC_ = COM_ = floating | | | 0.015 | 1 | µA |
| **ANALOG SWITCH** | | | | | | | |
| Analog Signal Range | | NO_, NC_, COM_ | | 0 | | $V_{CC}$ | V |
| On-Resistance | $R_{ON}$ | $V_{CC}$ = 2.7V, $I_{COM_}$ = 100mA, $V_{NO_}$ or $V_{NC_}$ = 0 to $V_{CC}$ (Note 3) | $T_A$ = +25°C | | 0.31 | 0.4 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 0.45 | |
| On-Resistance Match | $\Delta R_{ON}$ | $V_{CC}$ = 2.7V, $I_{COM_}$ = 100mA, $V_{NO_}$ or $V_{NC_}$ = 1.5V (Notes 3, 4) | $T_A$ = +25°C | | 0.015 | 0.03 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 0.03 | |
| On-Resistance Flatness | $R_{FLAT}$ | $V_{CC}$ = 2.7V; $I_{COM_}$ = 100mA; $V_{NO_}$ or $V_{NC_}$ = 0.6V, 1.2V, 1.8V (Note 5) | $T_A$ = +25°C | | 0.06 | 0.75 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 0.080 | |
| NO_ or NC_ Off-Leakage Current | $I_{OFF}$ | $V_{CC}$ = 3.3V; $V_{COM_}$ = 3V, 0.3V or floating; $V_{NO_}$ or $V_{NC_}$ = 0.3V, 3V or floating | $T_A$ = +25°C | 20 | | 20 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 100 | | 100 | |
| COM_ On-Leakage Current | $I_{ON}$ | $V_{CC}$ = 3.3V; $V_{NO_}$ or $V_{NC_}$ = 0.3V, 3V or floating; $V_{COM_}$ = 0.3V, 3V or floating | $T_A$ = +25°C | 20 | | 20 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 100 | | 100 | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 2.7V to 3.6V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = 3V, $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{CC}$ = 2.7V, $V_{NO_}$ or $V_{NC_}$ = 1.5V, $R_L$ = 50Ω, $C_L$ = 35pF, Figure 1 | $T_A$ = +25°C | | 40 | 200 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 200 | |
| Turn-Off Time | $t_{OFF}$ | $V_{CC}$ = 2.7V, $V_{NO_}$ or $V_{NC_}$ = 1.5V, $R_L$ = 50Ω, $C_L$ = 35pF, Figure 1 | $T_A$ = +25°C | | 20 | 180 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 180 | |
| Break-Before-Make Time | $t_{BBM}$ | $V_{CC}$ = 2.7V, $V_{NO_}$ or $V_{NC_}$ = 1.5V, $R_L$ = 50Ω, $C_L$ = 35pF, Figure 2 (Note 6) | $T_A$ = +25°C | 2 | 15 | | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 2 | | | |
| Charge Injection | Q | $V_{GEN}$ = 0V, $R_{GEN}$ = 0Ω, $C_L$ = 1nF, Figure 3 | | | 100 | | pC |
| On-Channel Bandwidth -3dB | BW | $R_L$ = 50Ω, Figure 4 | | | 20 | | MHz |
| Off-Isolation | $V_{ISO}$ | $V_{COM_}$ = 1$V_{RMS}$, $R_L$ = 50Ω, f = 100kHz, $C_L$ = 5pF, Figure 4 (Note 7) | | | -66 | | dB |
| Crosstalk | $V_{CT}$ | $V_{COM_}$ = 1$V_{RMS}$, $R_L$ = 50Ω, f = 100kHz, $C_L$ = 5pF, Figure 4 (Note 8) | | | -86 | | dB |
| Total Harmonic Distortion Plus Noise | THD+N | f = 20Hz to 20kHz; $V_{NC_}$, $V_{NO_}$, $V_{COM_}$ = 0.5$V_{P-P}$; $R_L$ = 32Ω | | | 0.02 | | % |
| NC_ or NO_ Off-Capacitance | $C_{NC_(OFF)}$, $C_{NO_(OFF)}$ | f = 1MHz, $V_{NO_}$ = $V_{NC_}$ = $V_{COM_}$ = 1.5V, Figure 5 | | | 70 | | pF |
| COM_ On-Capacitance | $C_{COM_(ON)}$ | f = 1MHz, $V_{NO_}$ = $V_{NC_}$ = $V_{COM_}$ = 1.5V, Figure 5 | | | 250 | | pF |
| Power-Supply Rejection Ratio | PSRR | $V_{AC}$ = 100m$V_{P-P}$, $V_{COM_}$ = 1.5V, $R_L$ = 50Ω, f = 100kHz | | | -34 | | dB |
| **DIGITAL INPUTS (INA,** | | | | | | | |
| Input-Logic High | $V_{IH}$ | | | 1.4 | | | V |
| Input-Logic Low | $V_{IL}$ | | | | | 0.5 | V |
| Input Leakage Current | $I_{IN}$ | $V_{IN_}$ = 0 or $V_{CC}$ | | | | ±200 | nA |

**Note 2:** Devices are 100% tested at $T_A$ = +85°C. Limits across the full temperature range are guaranteed by design and correlation.
**Note 3:** $R_{ON}$ and $R_{ON}$ matching specifications are guaranteed by design for MAX4735ETE only.
**Note 4:** $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
**Note 5:** Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over the specified analog signal ranges.
**Note 6:** Guaranteed by design, not production tested.
**Note 7:** Off-isolation = 20log10 [$V_{COM_}$ / ($V_{NO_}$ or $V_{NC_}$)], $V_{COM_}$ = output, $V_{NO_}$ or $V_{NC_}$ = input to off switch.
**Note 8:** Between any two switches.

# Low-Voltage, 0.31Ω, Quad-SPDT Analog Switch

## Timing Circuits/Timing Diagrams

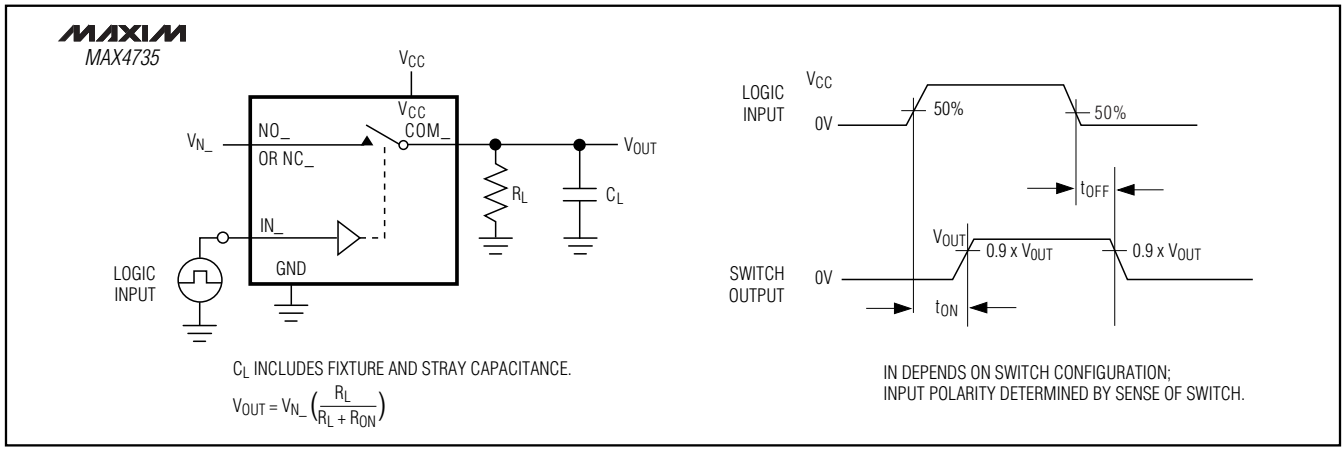



*Figure 1. Switching Time*

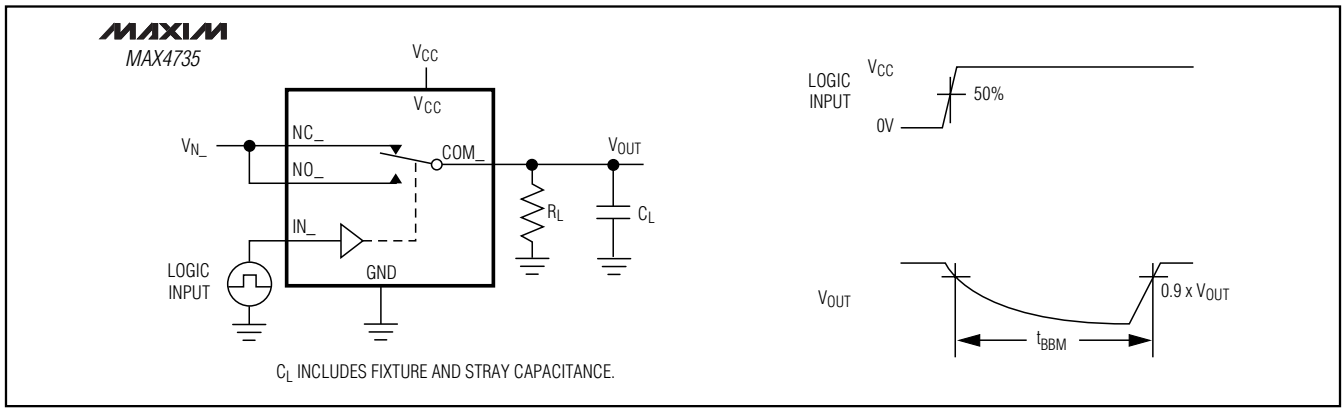



*Figure 2. Break-Before-Make Interval*

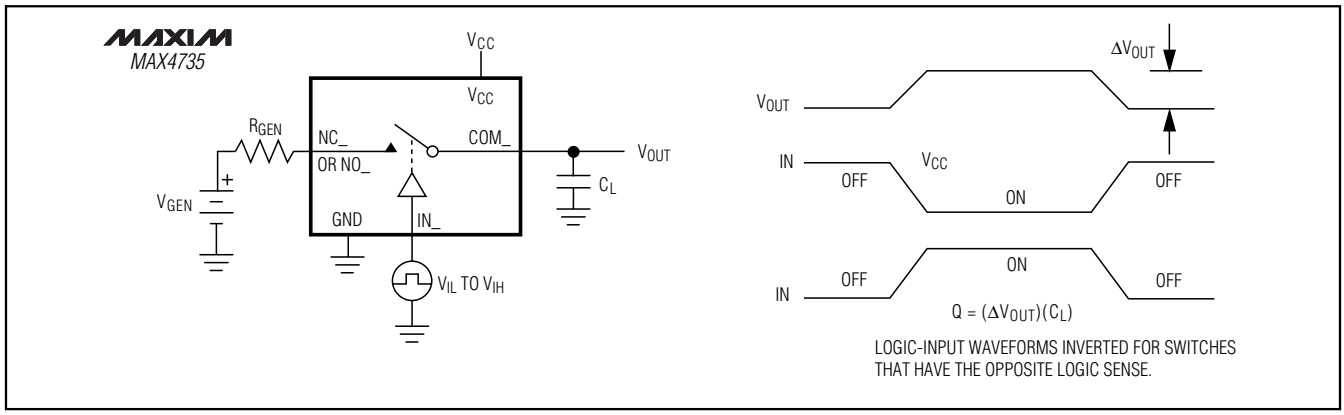



*Figure 3. Charge Injection*

## Timing Circuits/Timing Diagrams (continued)

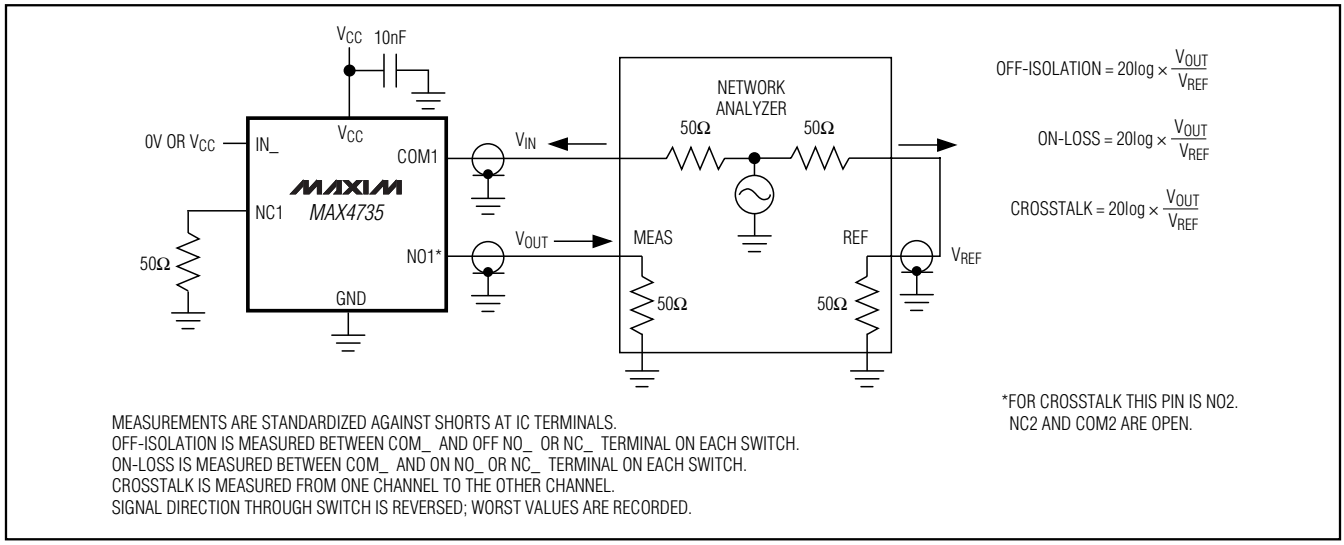



*Figure 4. On-Loss, Off-Isolation, and Crosstalk*

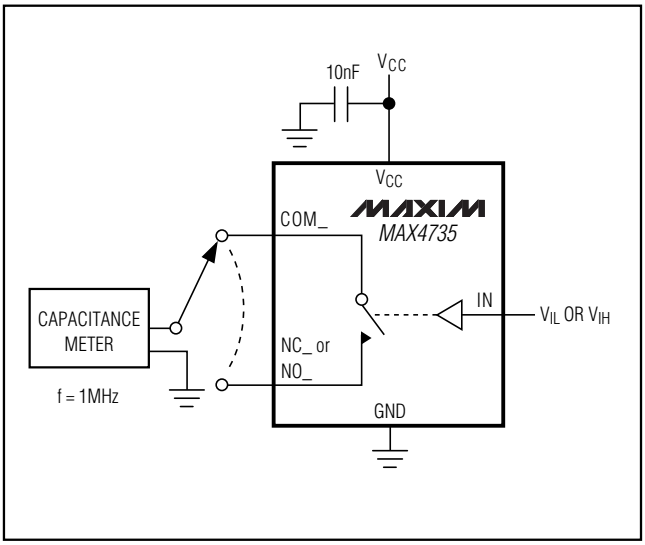


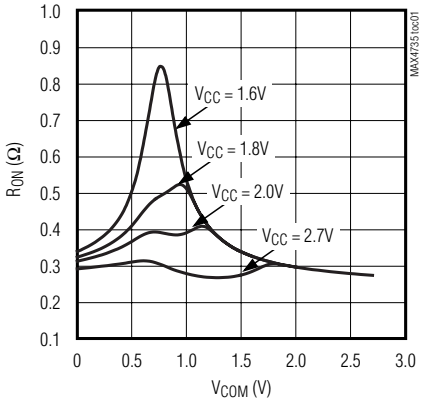

*Figure 5. Channel On-/Off-Capacitance*

# Low-Voltage, 0.31Ω, Quad-SPDT Analog Switch

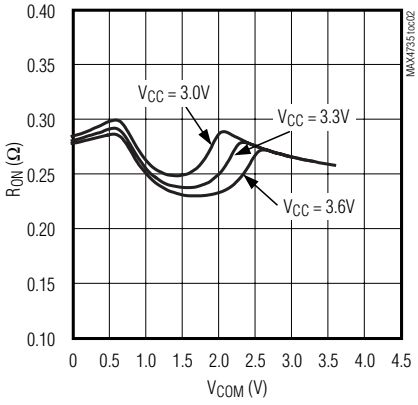
## Typical Operating Characteristics

($V_{CC}$ = 3V, $T_A$ = +25°C, unless otherwise noted.)

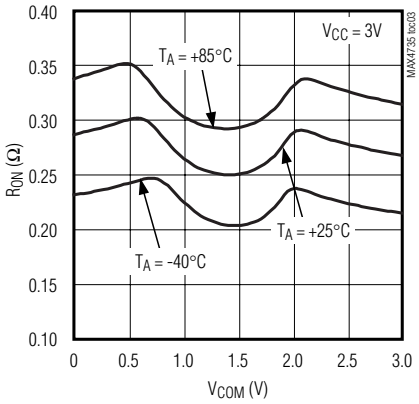
**ON-RESISTANCE vs. COM_ VOLTAGE**



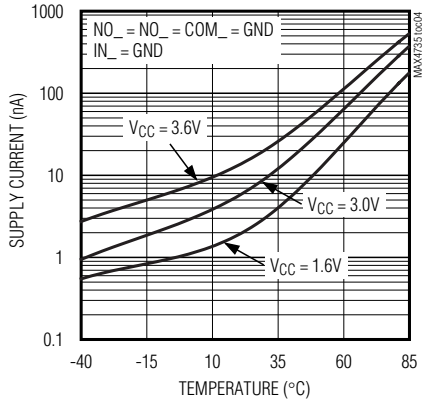

**ON-RESISTANCE vs. COM_ VOLTAGE**



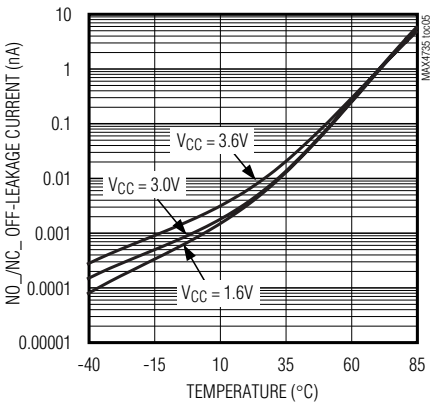

**ON-RESISTANCE vs. COM_ VOLTAGE AND TEMPERATURE**



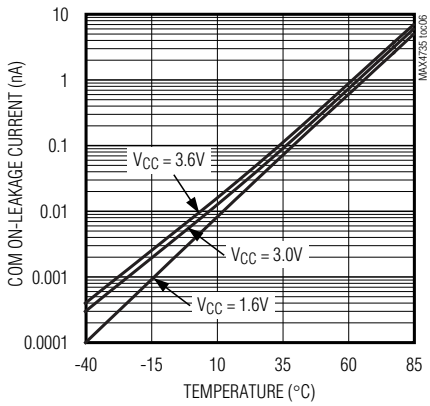

**SUPPLY CURRENT vs. TEMPERATURE**



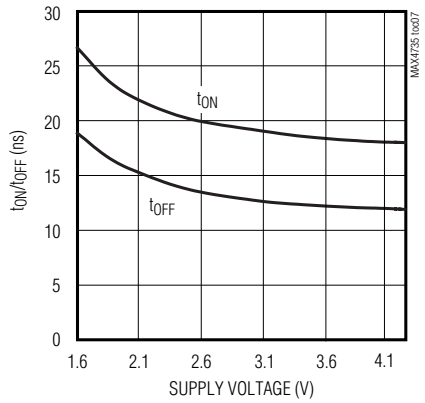

**NO_/NC_ OFF-LEAKAGE CURRENT vs. TEMPERATURE**



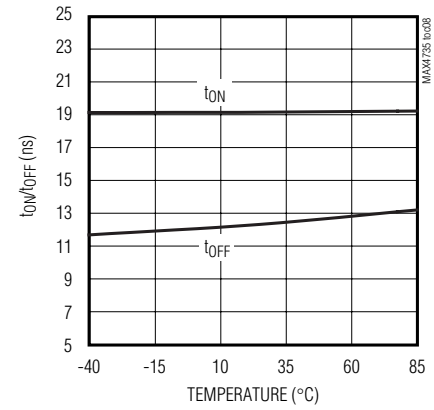

**COM_ ON-LEAKAGE CURRENT vs. TEMPERATURE**



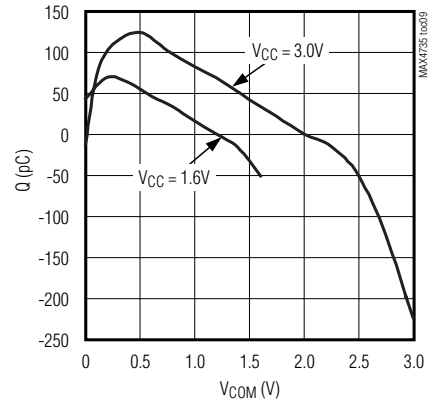

**TURN-ON/OFF TIME vs. SUPPLY VOLTAGE**




**TURN-ON/OFF TIME vs. TEMPERATURE**



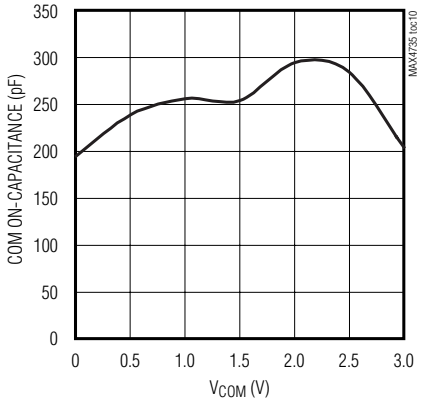

**CHARGE INJECTION vs. COM_ VOLTAGE**



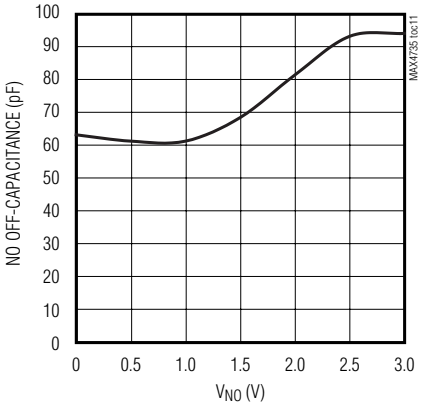
## Typical Operating Characteristics (continued)

($V_{CC}$ = 3V, $T_A$ = +25°C, unless otherwise noted.)

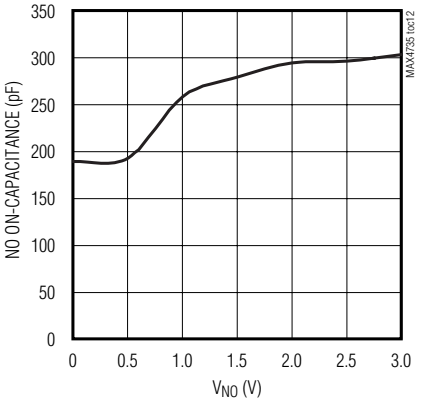
**COM_ ON-CAPACITANCE vs. COM_ VOLTAGE**



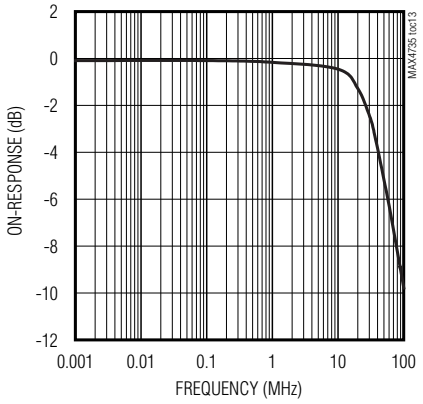

**NO_ OFF-CAPACITANCE vs. NO_ VOLTAGE**



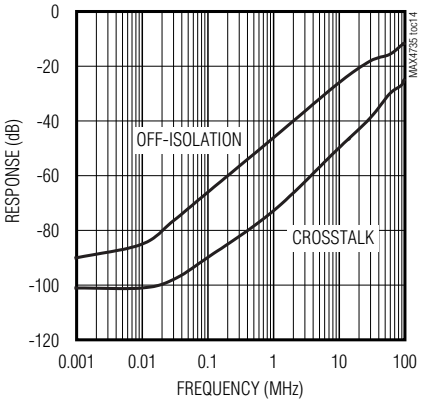

**NO_ ON-CAPACITANCE vs. NO_ VOLTAGE**



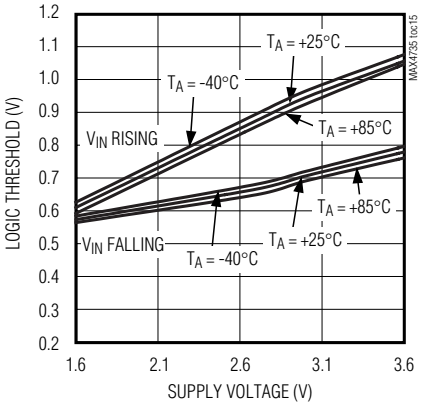

**ON-RESPONSE vs. FREQUENCY**



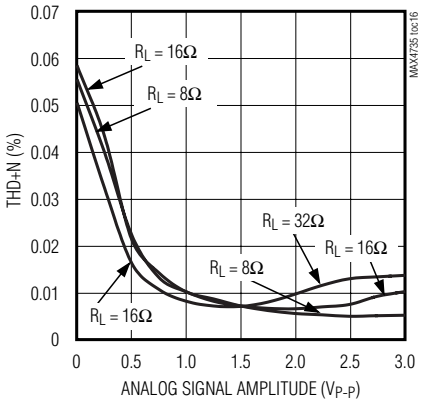

**OFF-ISOLATION AND CROSSTALK vs. FREQUENCY**



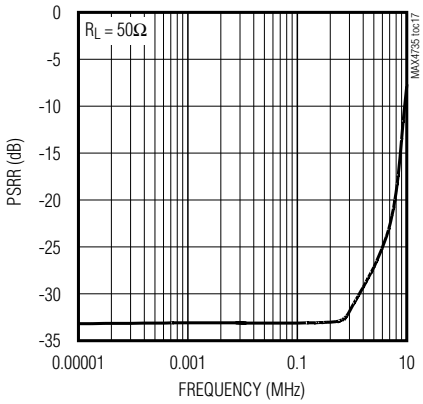

**LOGIC THRESHOLD vs. SUPPLY VOLTAGE**




**TOTAL HARMONIC DISTORTION PULSE NOISE vs. SIGNAL AMPLITUDE**




**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY**



# Low-Voltage, 0.31Ω, Quad-SPDT Analog Switch

## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| TSSOP | TQFN | | |
| 1 | 15 | INA | Select Input A. Controls switch 1 and switch 2. |
| 2 | 16 | NC1 | Normally Closed Terminal Switch 1 |
| 3 | 1 | COM1 | Common Terminal Switch 1 |
| 4 | 2 | NO1 | Normally Open Terminal Switch 1 |
| 5 | 3 | NC2 | Normally Closed Terminal Switch 2 |
| 6 | 4 | COM2 | Common Terminal Switch 2 |
| 7 | 5 | NO2 | Normally Open Terminal Switch 2 |
| 8 | 6 | GND | Ground |
| 9 | 7 | INB | Select Input B. Controls switch 3 and switch 4. |
| 10 | 8 | NO3 | Normally Open Terminal Switch 3 |
| 11 | 9 | COM3 | Common Terminal Switch 3 |
| 12 | 10 | NC3 | Normally Closed Terminal Switch 3 |
| 13 | 11 | NO4 | Normally Open Terminal Switch 4 |
| 14 | 12 | COM4 | Common Terminal Switch 4 |
| 15 | 13 | NC4 | Normally Closed Terminal Switch 4 |
| 16 | 14 | $V_{CC}$ | Positive Power Supply |
| — | PAD | EP | Exposed Pad. Connect to GND. |

## Detailed Description

The MAX4735 quad-SPDT analog switch operates from a single +1.6V to +3.6V supply. These devices are fully specified for +3V applications.

The MAX4735 features fully bidirectional, rail-to-rail CMOS analog switch channels. They can be configured as dual-DPDT switches, dual 4:2 multiplexers/demultiplexers, or as a single 8:4 multiplexer/demultiplexer. See Figure 6.

## Applications Information

### Analog Signal Range

The CMOS switches in the MAX4735 function on any signal within the power-supply voltages. If any channel exceeds $V_{CC}$, it is clamped to $V_{CC}$ by a silicon diode. If any channel goes below GND, it is clamped to GND by a silicon diode. Ensure that if either of these diodes becomes forward biased, the continuous and peak currents do not exceed those listed in the *Absolute Maximum Ratings* section of this data sheet.

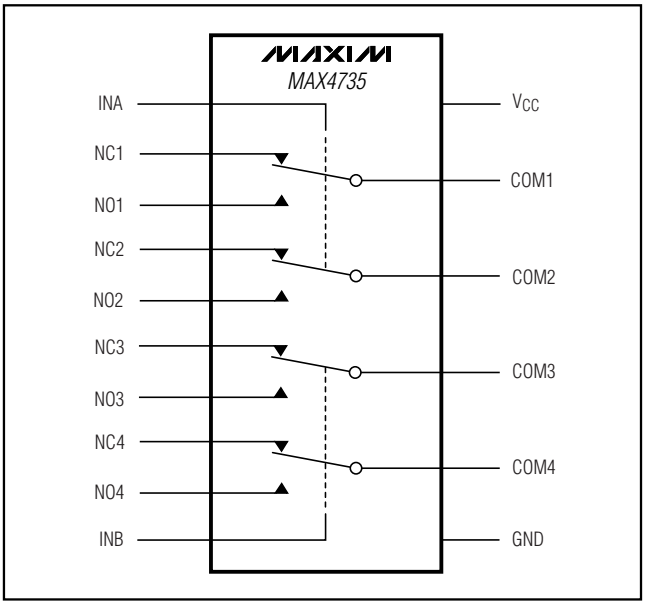



*Figure 6. Functional Diagram*

As seen in the *Typical Operating Characteristics*, the on-resistance of the MAX4735 is inversely proportional to the supply voltage. Best performance is obtained by using the highest supply voltage available within the +1.6V to +3.6V range.

### Digital Logic Inputs

Digital control inputs INA and INB control the position of the switches in the MAX4735. These inputs are diode clamped to GND only. It is acceptable to leave these pins driven in the absence of a $V_{CC}$ power supply.

For best performance, drive INA and INB to the full supply voltage range of the MAX4735.

The two switch sections of the MAX4735 operate independently. Drive INA low to connect COM1 to NC1 and connect COM2 to NC2. Drive INA high to connect COM1 to NO1 and connect COM2 to NO2. Drive INB low to connect COM3 to NC3 and connect COM4 to NC4. Drive INB high to connect COM3 to NO3 and connect COM4 to NO4. See Table 1.

INA and INB have typical hystersis of 100mV by including positive feedback in the internal buffer. Thus, for applications using DC or very slow ramp rate of the digital input voltage level, connect a 100pF capacitor from IN_ to GND to limit the $I_{CC}$ current at the trip point. The switching point is typically 0.7V between $V_{IL}$ and $V_{IH}$ levels.

### Power Supply

The MAX4735 operates from a +1.6V to +3.6V power supply. For best results, bypass $V_{CC}$ to GND with a 0.1µF ceramic chip capacitor located close to the IC.

### Audio Signal Routing

The MAX4735's low $R_{ON}$ makes it an excellent choice for multiplexing loudspeakers in portable equipment. THD performance is inversely proportional to load impedance. Within the audio signal range, there is no frequency component to THD. The only distortion mechanism is the $R_{ON}$ flatness' modulation of the signal into a load. Therefore, for best distortion performance, use higher impedance transducers.

**Table 1. Truth Table**

| INA | INB | SWITCH 1 AND SWITCH 2 STATE | SWITCH 3 AND SWITCH 4 STATE |
|---|---|---|---|
| 0 | — | COM1 to NC1<br>COM2 to NC2 | — |
| 1 | — | COM1 to NO1<br>COM2 to NO2 | — |
| — | 0 | — | COM3 to NC3<br>COM4 to NC4 |
| — | 1 | — | COM3 to NO3<br>COM4 to NO4 |

Each switch channel on the MAX4735 has an absolute maximum rating 300mA continuous current, and 400mA peak current at 50% duty cycle. When driving low-impedance loudspeakers, the peak signal amplitude should be limited so these peak currents are not exceeded. For an 8Ω load, this corresponds to $2.3V_{RMS}$. For a 4Ω load, this is $1.1V_{RMS}$.

### Package Information

The MAX4735 is offered in 16-pin TSSOP and 3mm x 3mm x 0.8mm TQFN packages. The mechanical drawings for these packages are located at the end of this data sheet. Please check www.maxim-ic.com/packages to ensure working with the latest information.

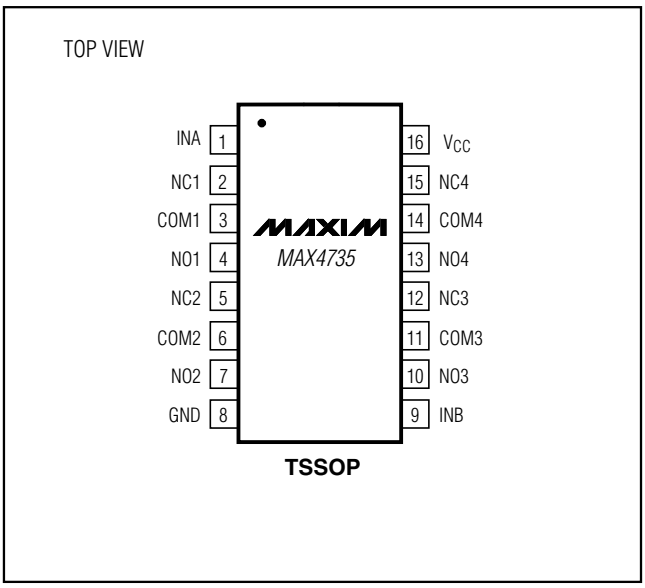
The TSSOP package is rated for a peak power dissipation of 755mW at +70°C, with a $\theta_{JA}$ of 106°C/W on a single-layer PC board. The TQFN package is rated for a peak power dissipation of 1.25W at +70°C, with a $\theta_{JA}$ of 64°C/W on a single-layer PC board. The TQFN package is the T1633-4 package code variant.

# Low-Voltage, 0.31Ω, Quad-SPDT Analog Switch

## Chip Information

TRANSISTOR COUNT: 487
PROCESS: CMOS

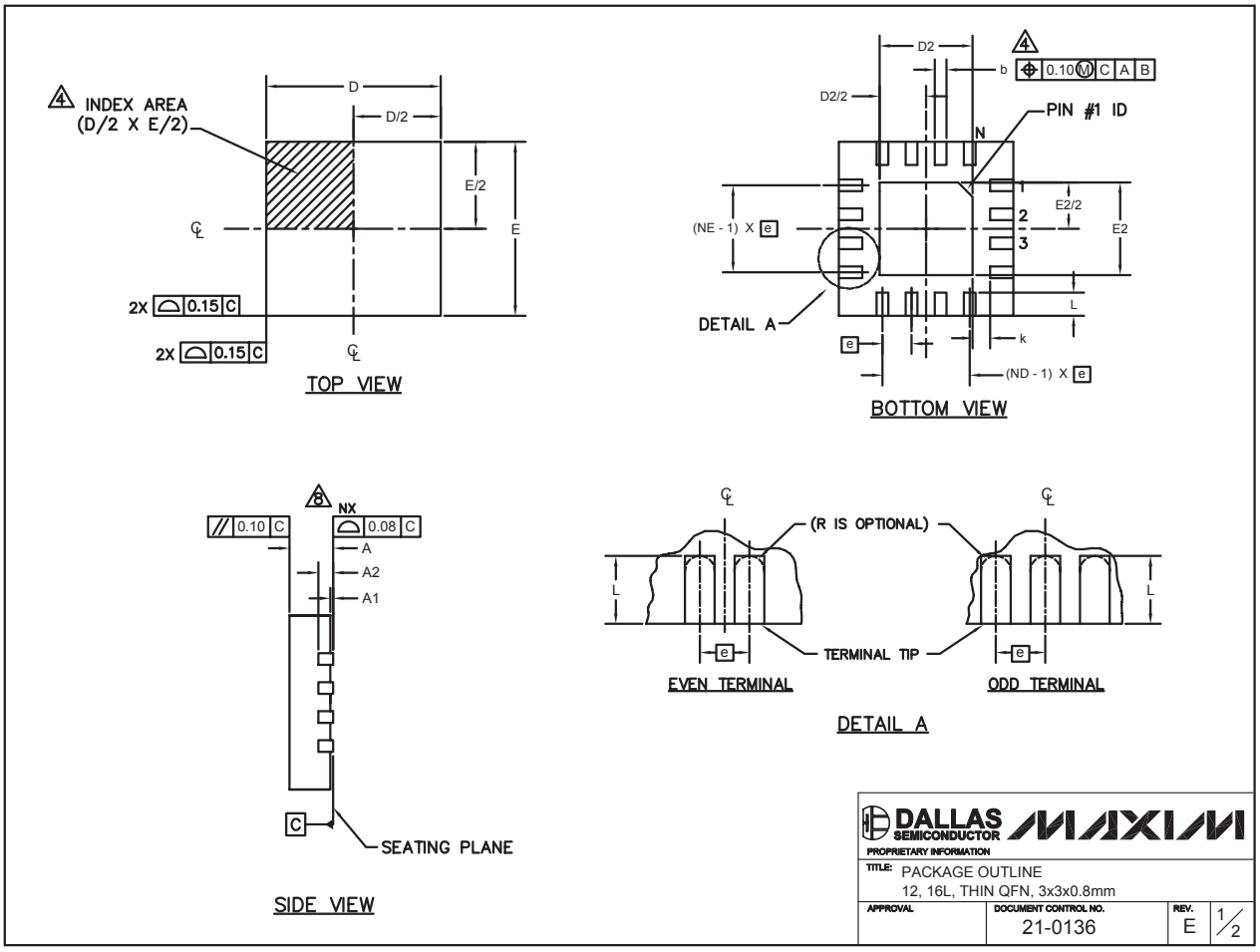
## Pin Configurations (continued)



## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



# Low-Voltage, 0.31Ω, Quad-SPDT Analog Switch

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

| PKG | 12L 3x3 | | | 16L 3x3 | | |
|---|---|---|---|---|---|---|
| REF. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| b | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 |
| D | 2.90 | 3.00 | 3.10 | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 | 2.90 | 3.00 | 3.10 |
| e | 0.50 BSC. | | | 0.50 BSC. | | |
| L | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | |
| ND | 3 | | | 4 | | |
| NE | 3 | | | 4 | | |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 |
| A2 | 0.20 REF | | | 0.20 REF | | |
| k | 0.25 | - | - | 0.25 | - | - |

EXPOSED PAD VARIATIONS

| PKG. CODES | D2 | | | E2 | | | PIN ID | JEDEC | DOWN BONDS ALLOWED |
|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | | | |
| T1233-1 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45∞ | WEED-1 | NO |
| T1233-3 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45∞ | WEED-1 | YES |
| T1633-1 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45∞ | WEED-2 | NO |
| T1633-2 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45∞ | WEED-2 | YES |
| T1633F-3 | 0.65 | 0.80 | 0.95 | 0.65 | 0.80 | 0.95 | 0.225 x 45∞ | WEED-2 | N/A |
| T1633-4 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45∞ | WEED-2 | NO |

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

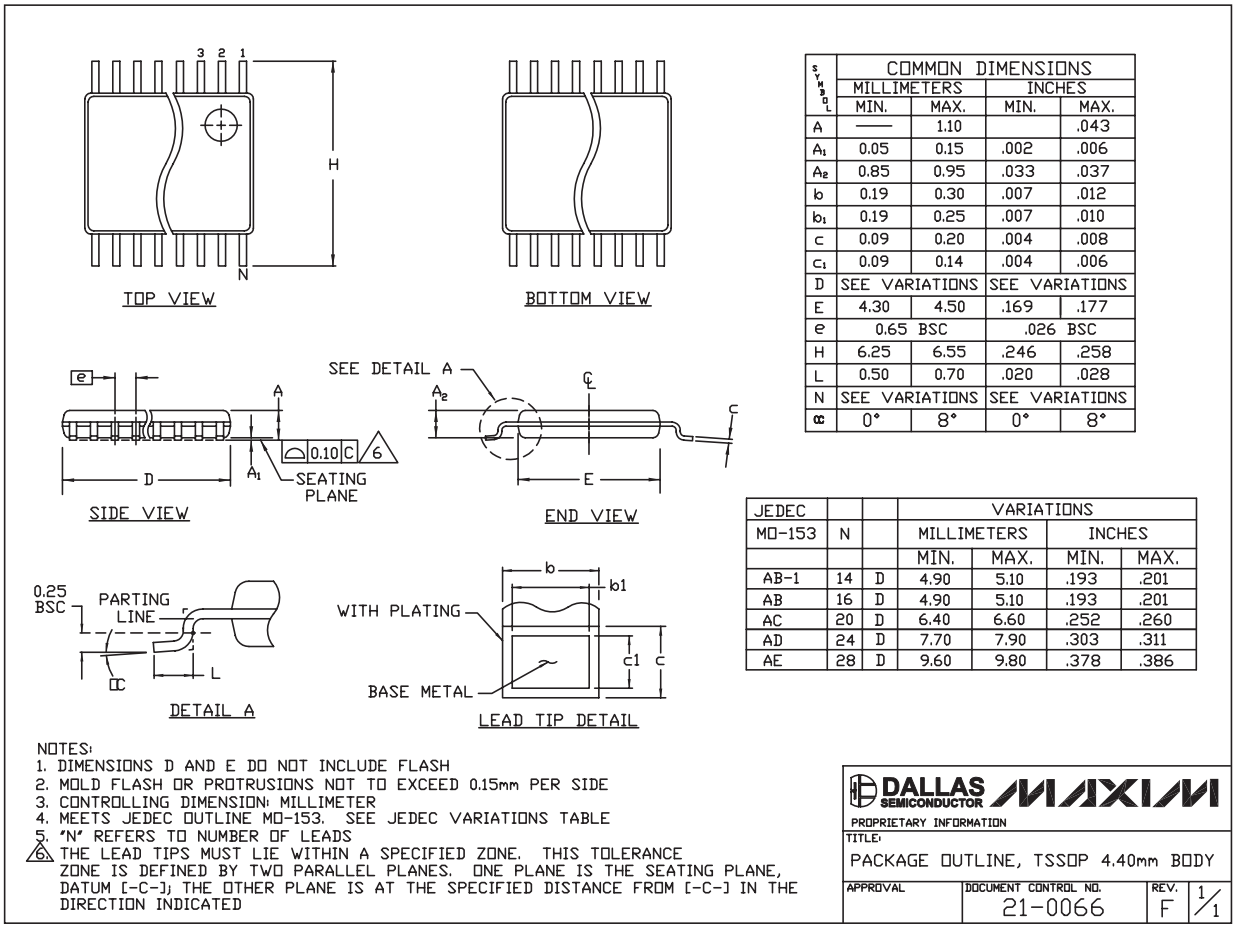
TITLE: PACKAGE OUTLINE
12, 16L, THIN QFN, 3x3x0.8mm

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0136 | E | 2/2 |

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS




| SYMBOL | COMMON DIMENSIONS | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | —— | 1.10 | | .043 |
| $A_1$ | 0.05 | 0.15 | .002 | .006 |
| $A_2$ | 0.85 | 0.95 | .033 | .037 |
| b | 0.19 | 0.30 | .007 | .012 |
| $b_1$ | 0.19 | 0.25 | .007 | .010 |
| c | 0.09 | 0.20 | .004 | .008 |
| $c_1$ | 0.09 | 0.14 | .004 | .006 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BSC | | .026 BSC | |
| H | 6.25 | 6.55 | .246 | .258 |
| L | 0.50 | 0.70 | .020 | .028 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

| JEDEC | | | VARIATIONS | | | |
|---|---|---|---|---|---|---|
| MO-153 | N | | MILLIMETERS | | INCHES | |
| | | | MIN. | MAX. | MIN. | MAX. |
| AB-1 | 14 | D | 4.90 | 5.10 | .193 | .201 |
| AB | 16 | D | 4.90 | 5.10 | .193 | .201 |
| AC | 20 | D | 6.40 | 6.60 | .252 | .260 |
| AD | 24 | D | 7.70 | 7.90 | .303 | .311 |
| AE | 28 | D | 9.60 | 9.80 | .378 | .386 |

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0066 | F | 1/1 |


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